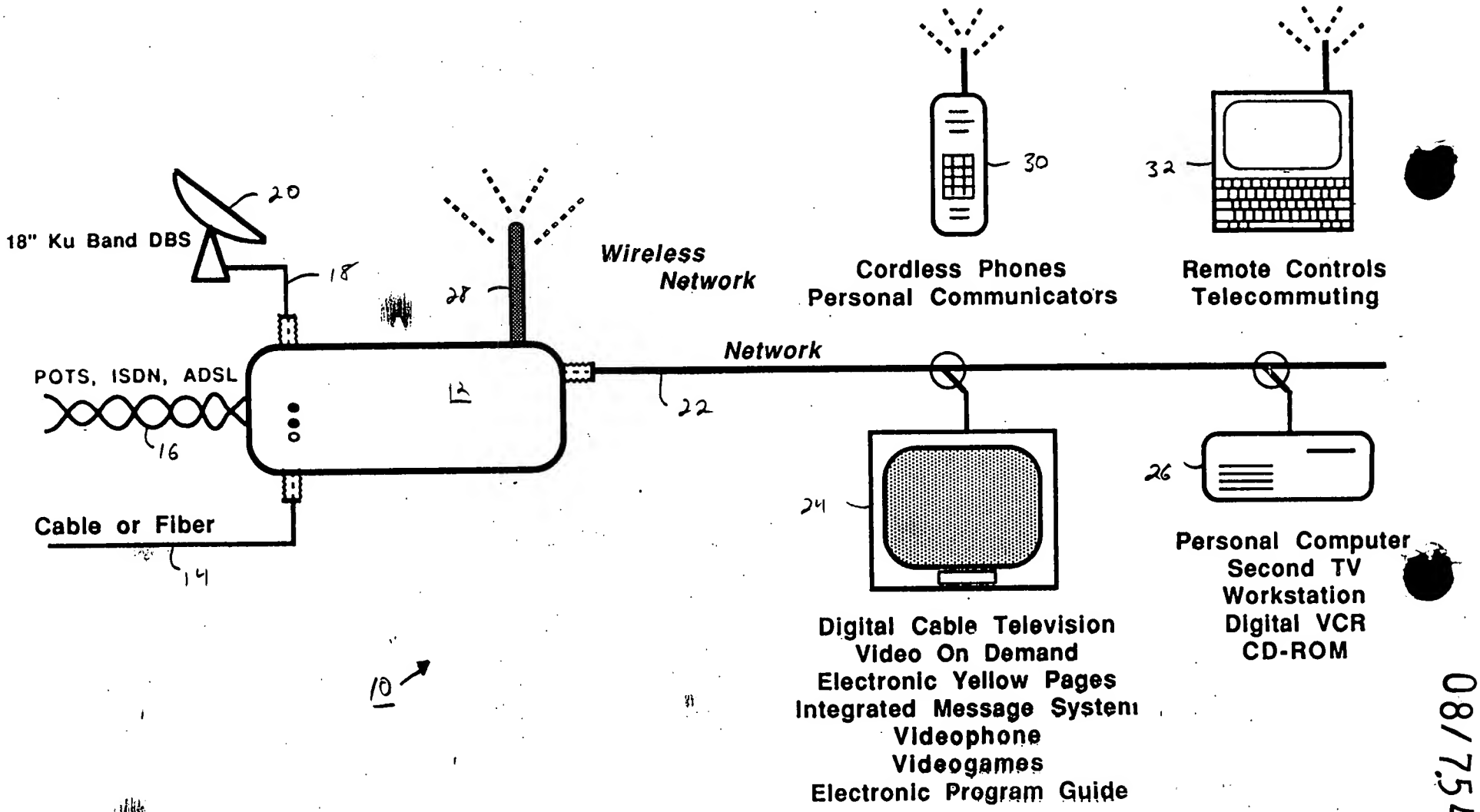
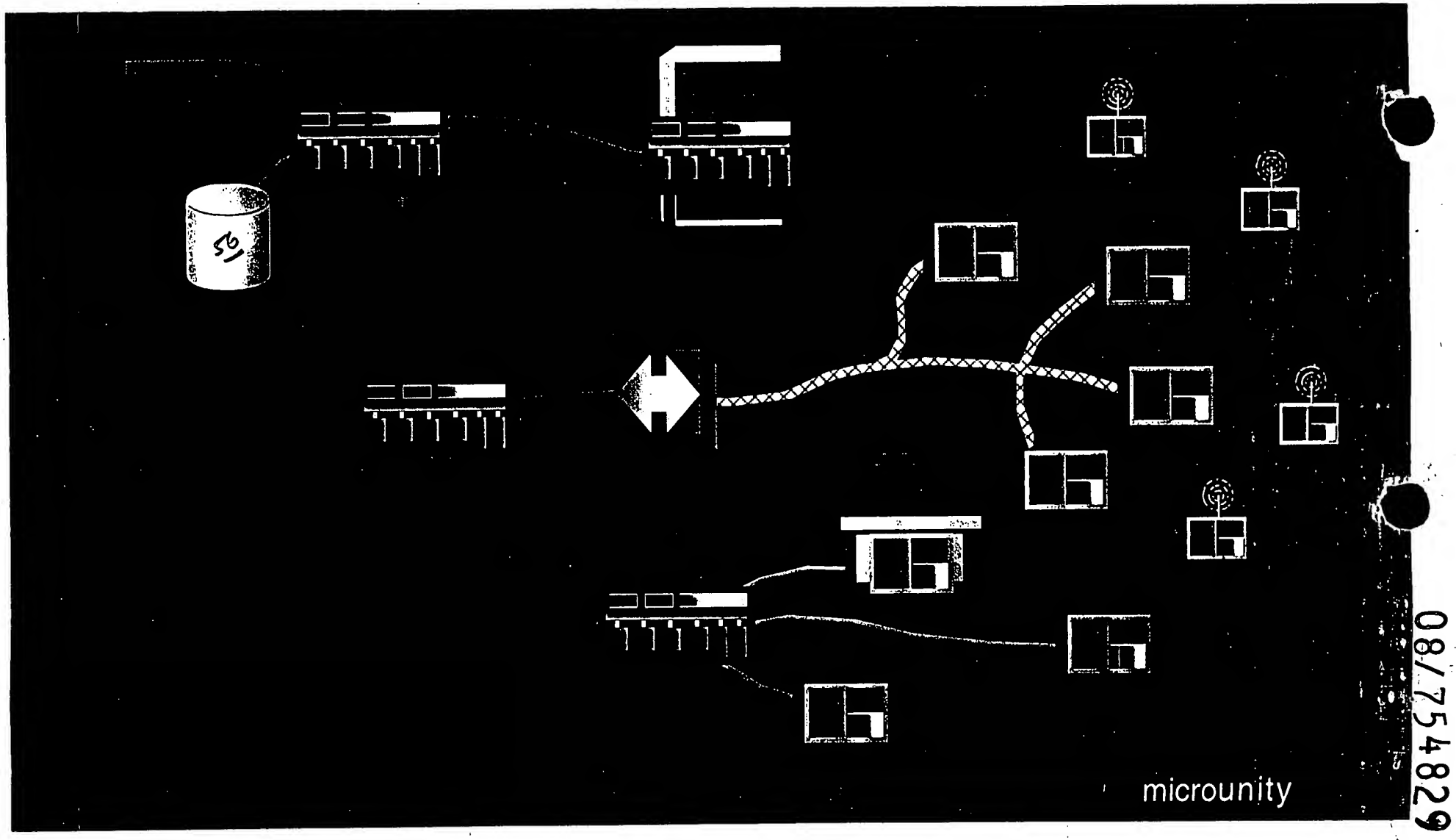


Figure 1

31

Figure 2



08/754829

Figure3

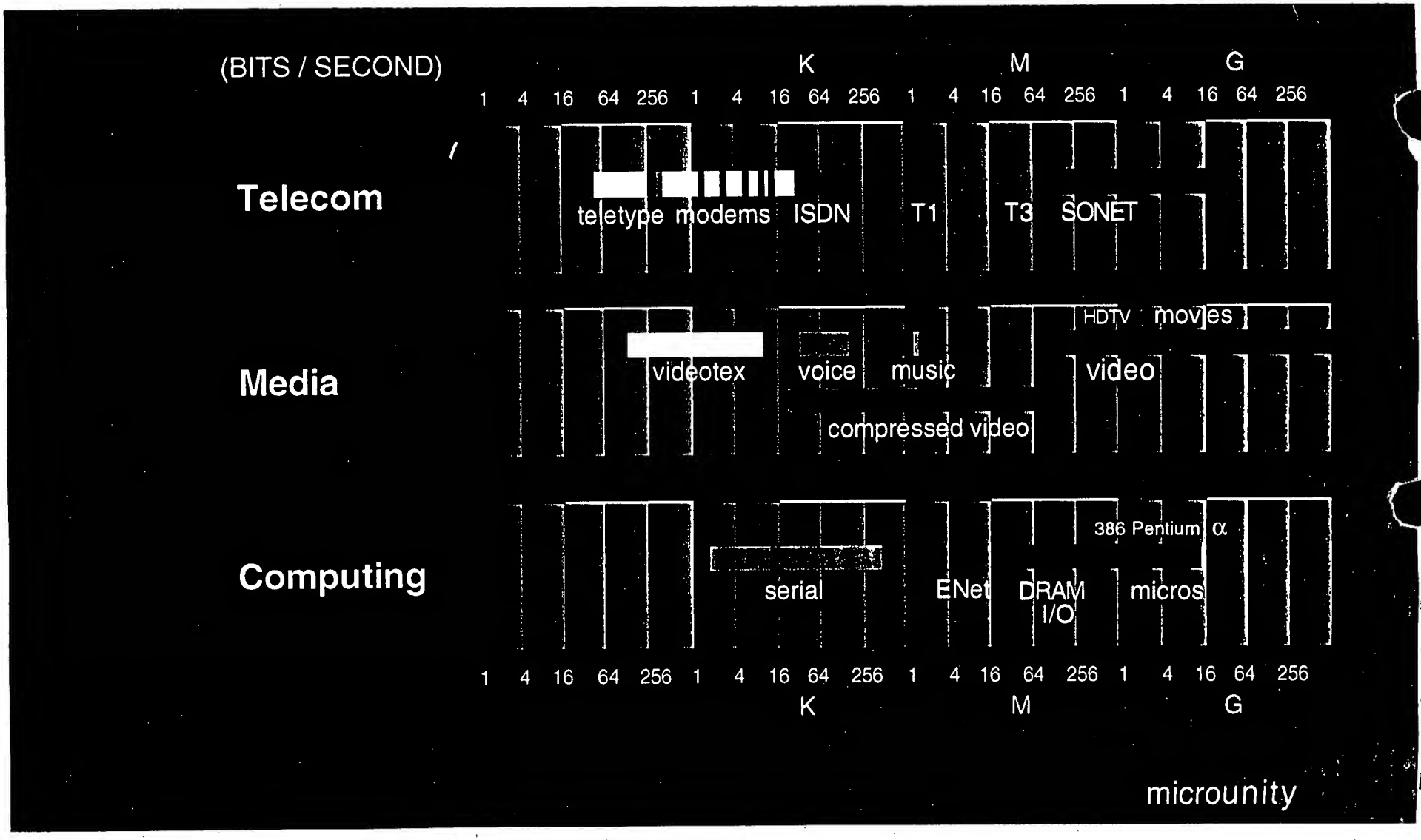


Figure 4

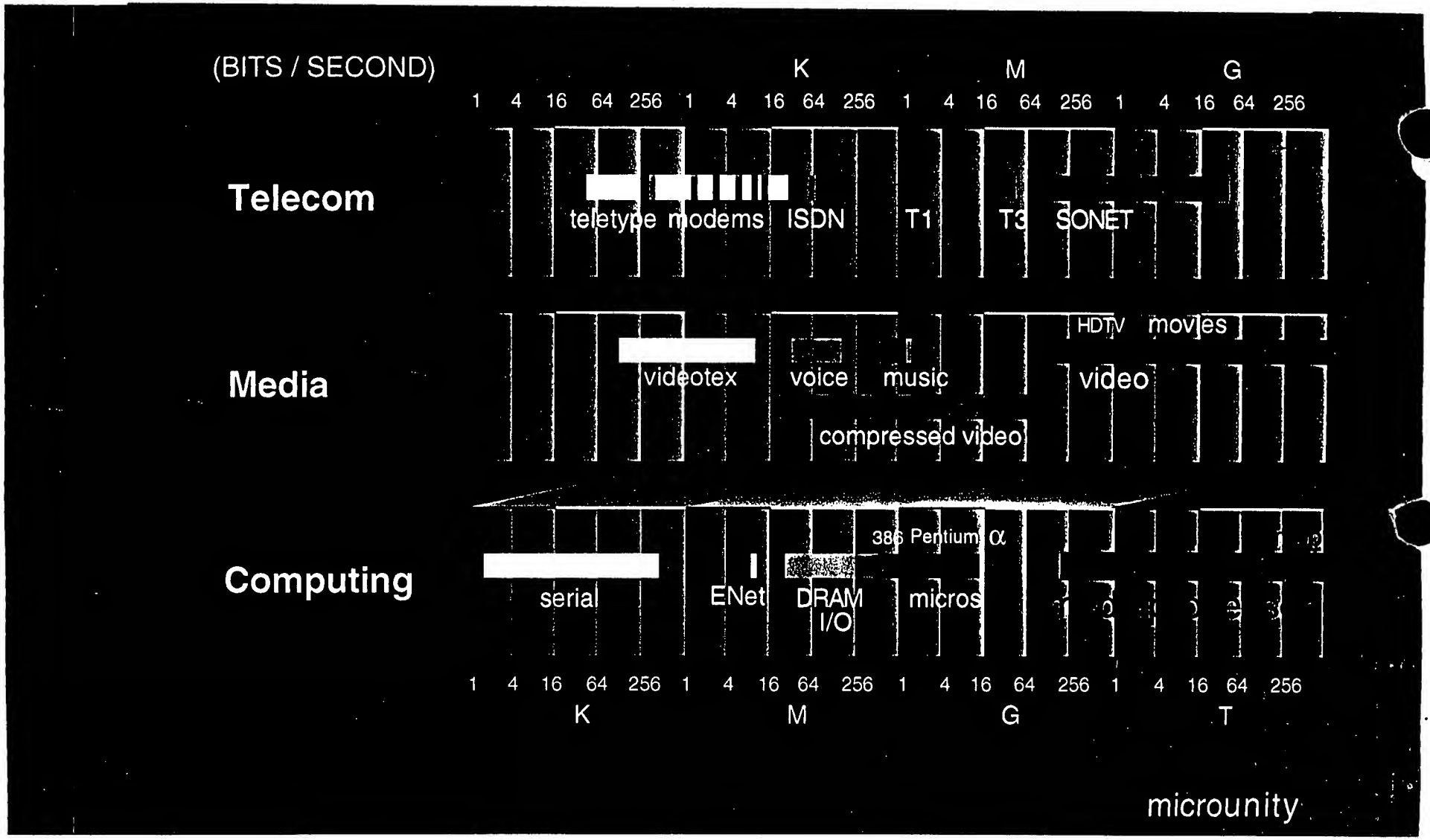


Figure 5

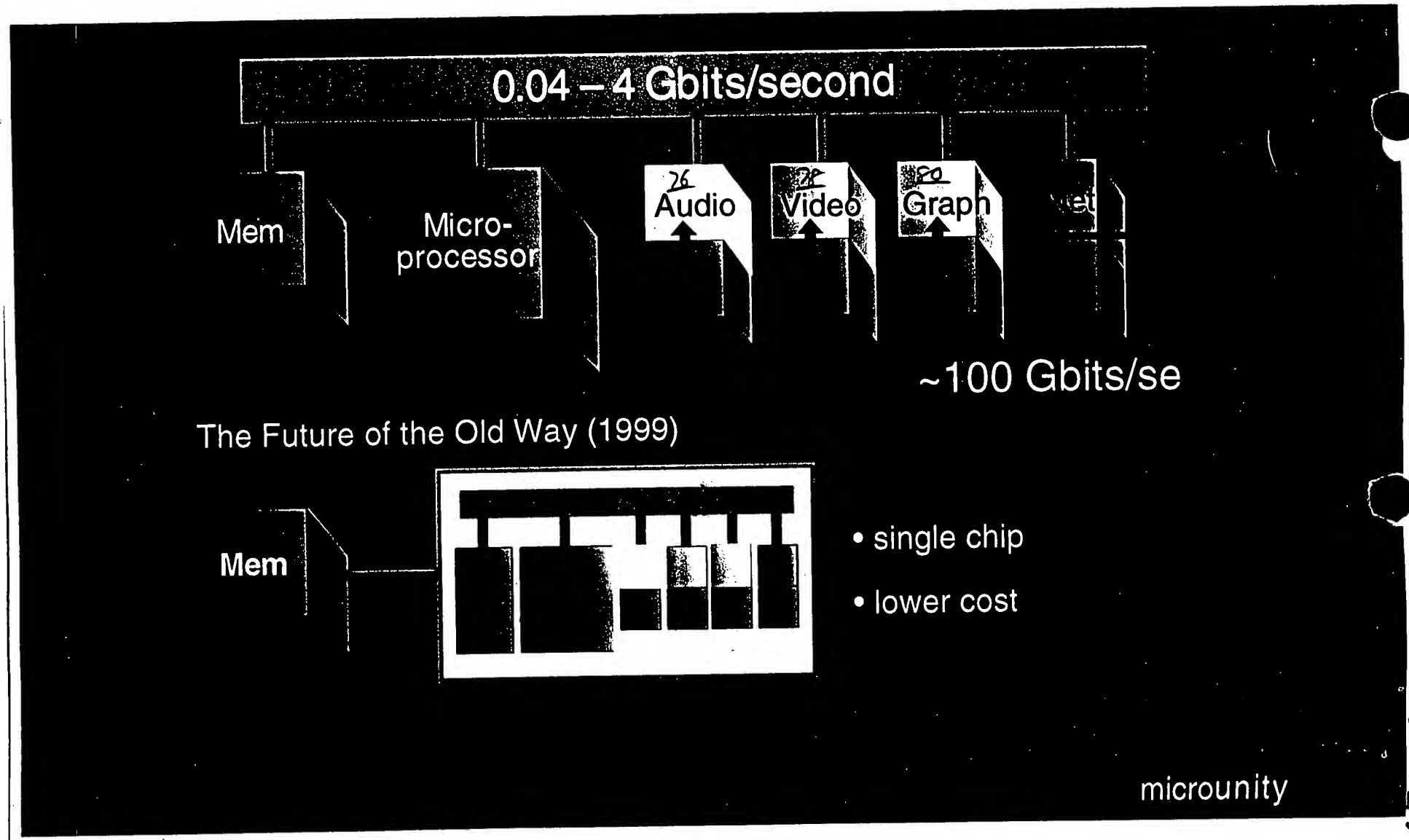
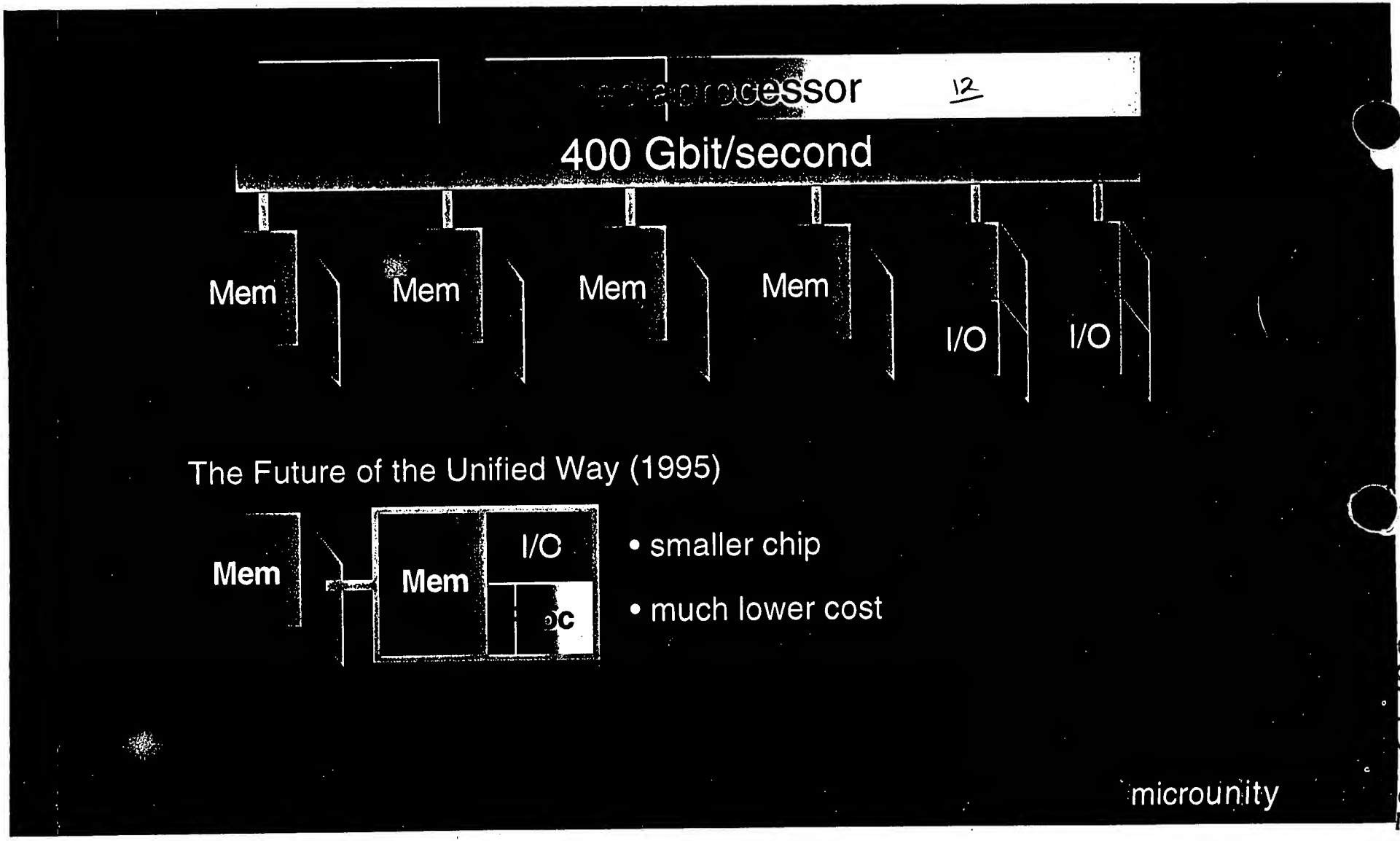


Figure 6



08/754829

Figure 7

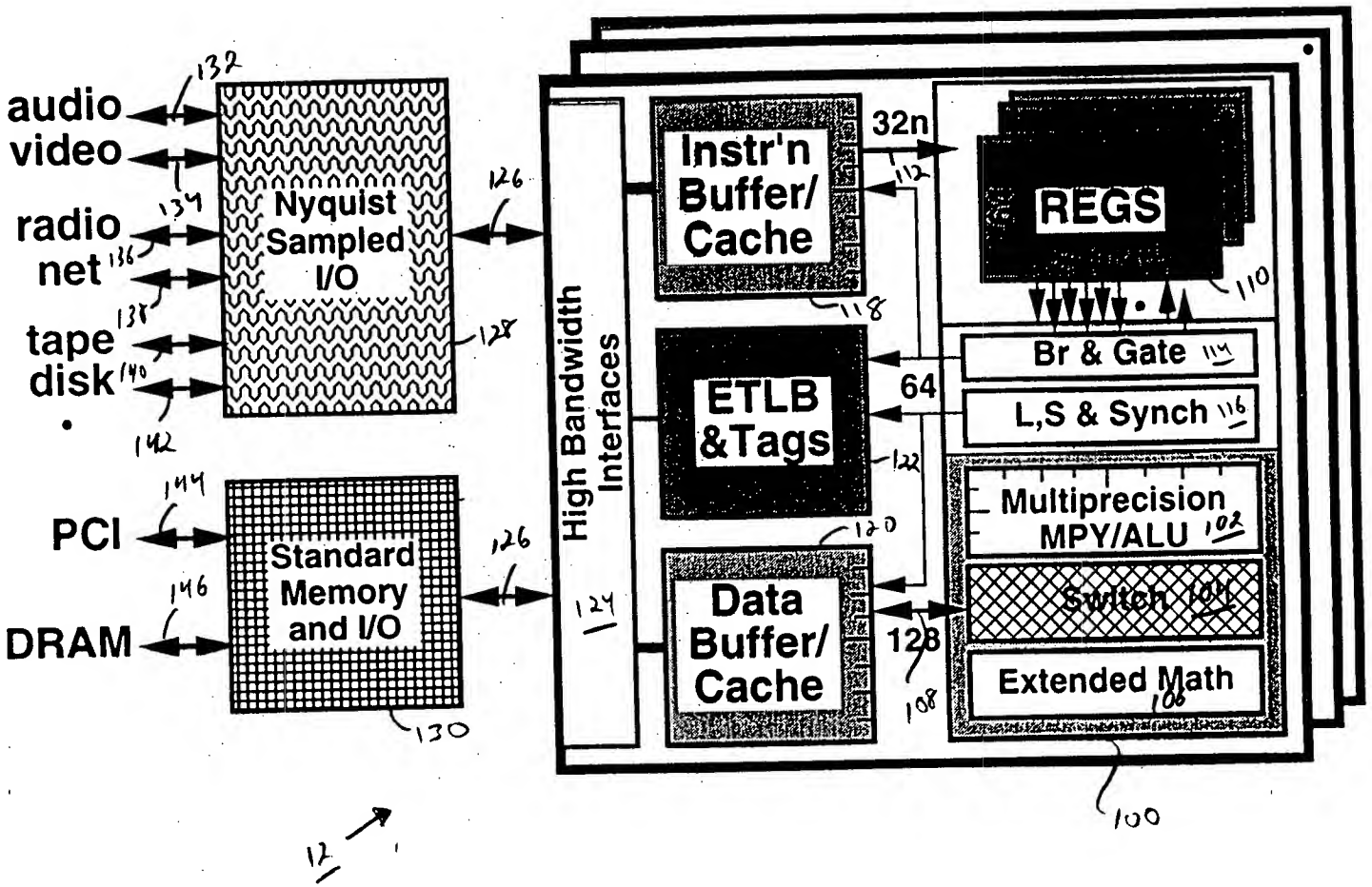


Figure 8(a)

Group Expand

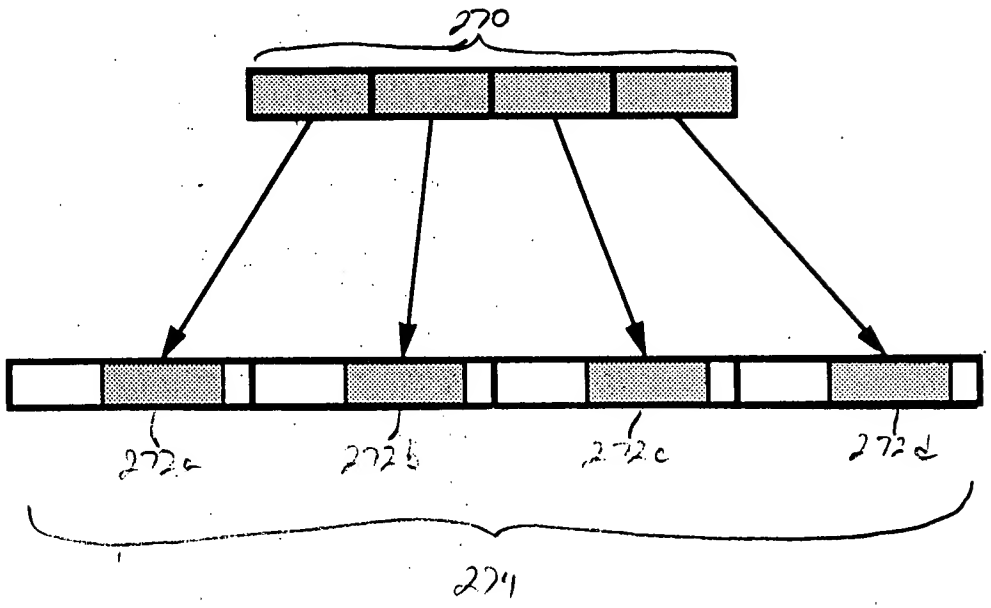


Figure 8(b)

Group Compress, Extract

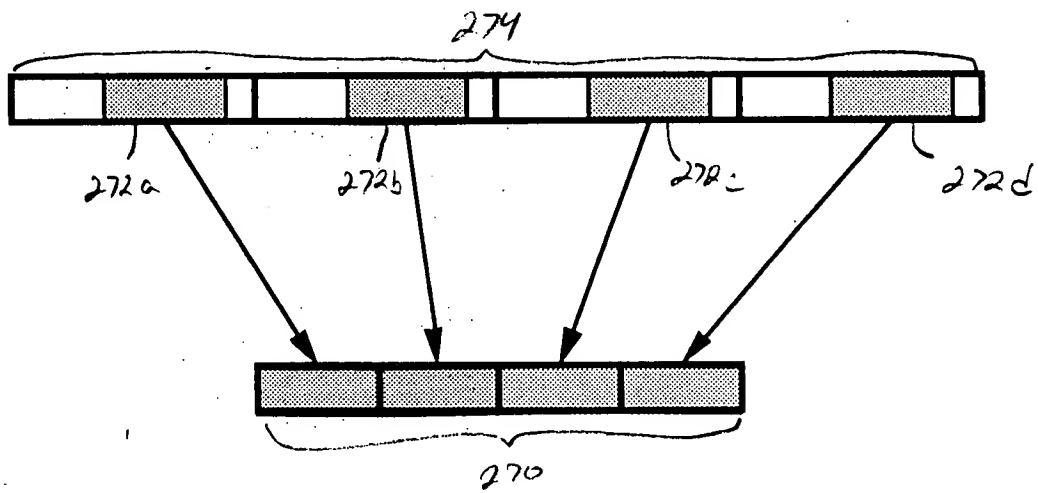
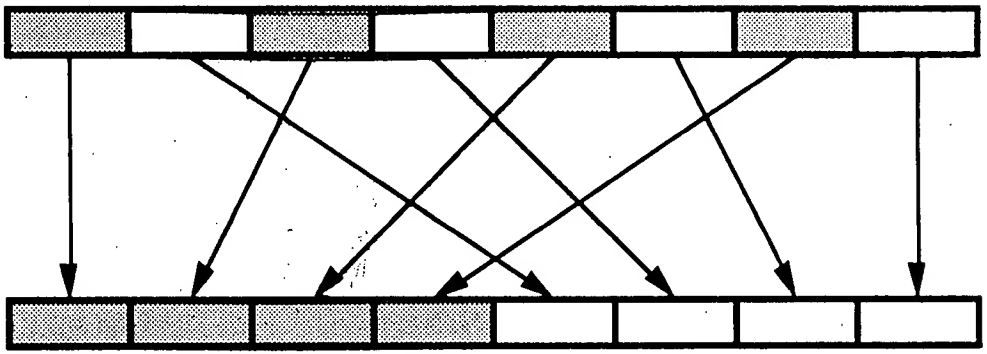


Figure 8(c)

Group Deal, Shuffle

- Group Deal: 128 bits to 128 bits



- Group Shuffle: 128 bits to 128 bits

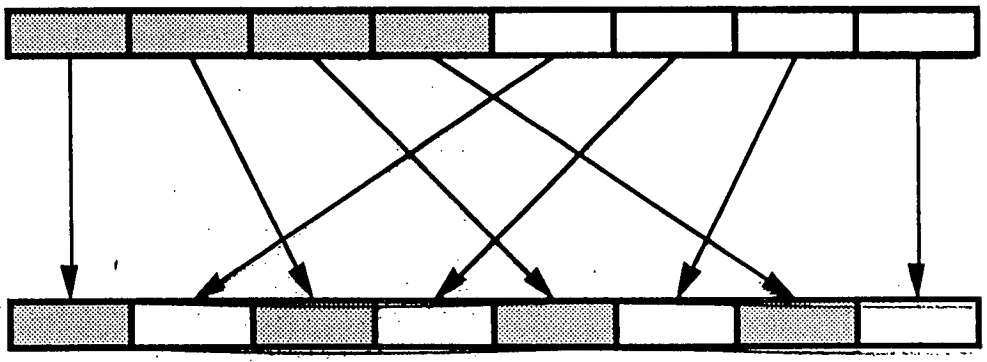


Figure 8(d)

Group Swizzle (Copy-Swap)

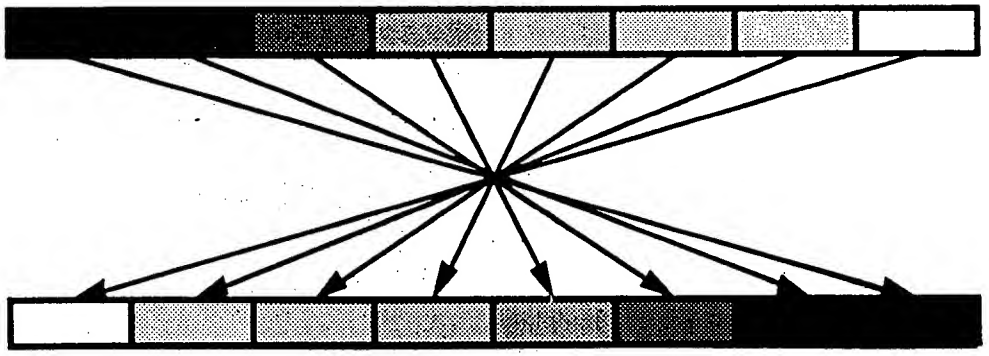
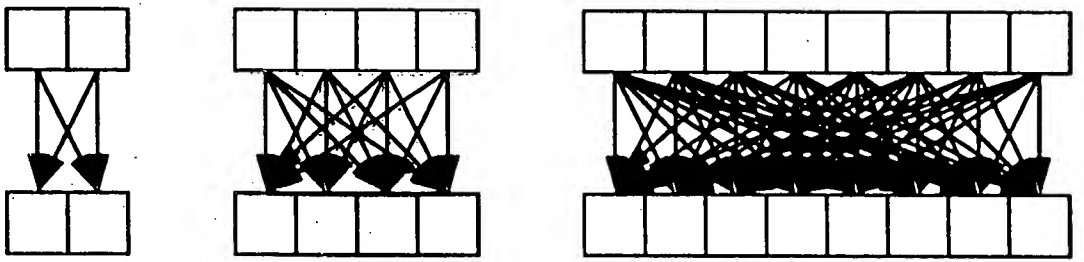


Figure 8(e)

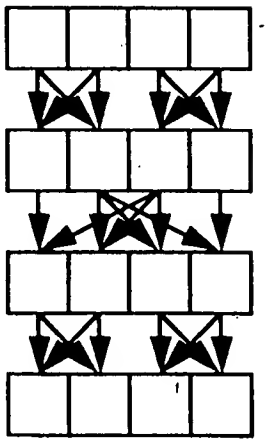
Group Permute

2-mux 4-mux 8-mux

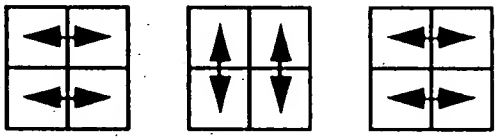


Benes network: multistage permutation

4-mux, 3 stage



4-mux, two-dimensional (3-stage)



16-mux, two-dimensional (3-stage)

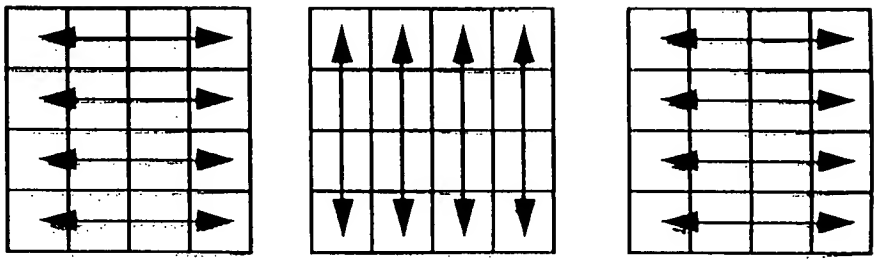


Figure 9(a)

Instruction Formats

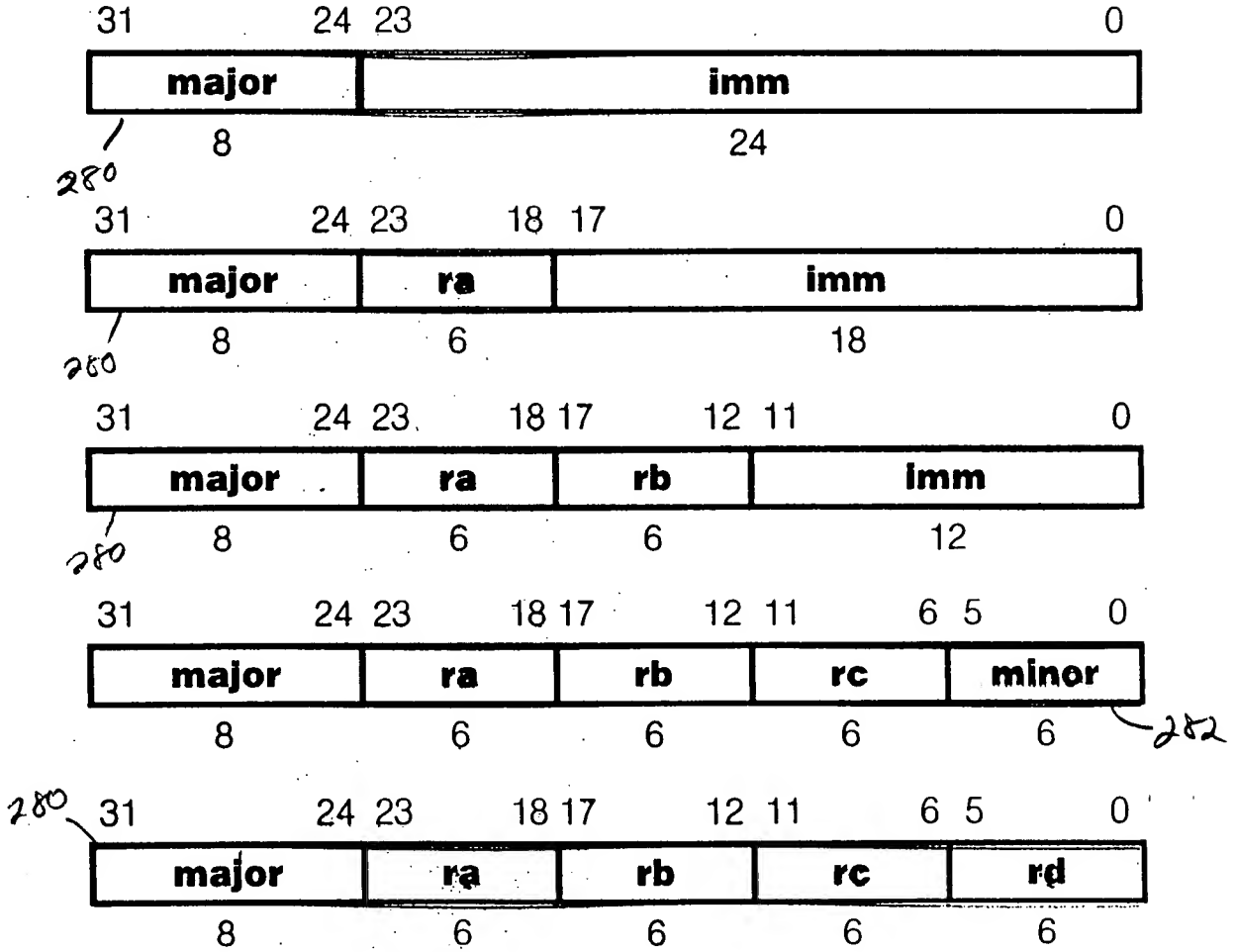


Figure 9(b)

Floating-point Data Sizes

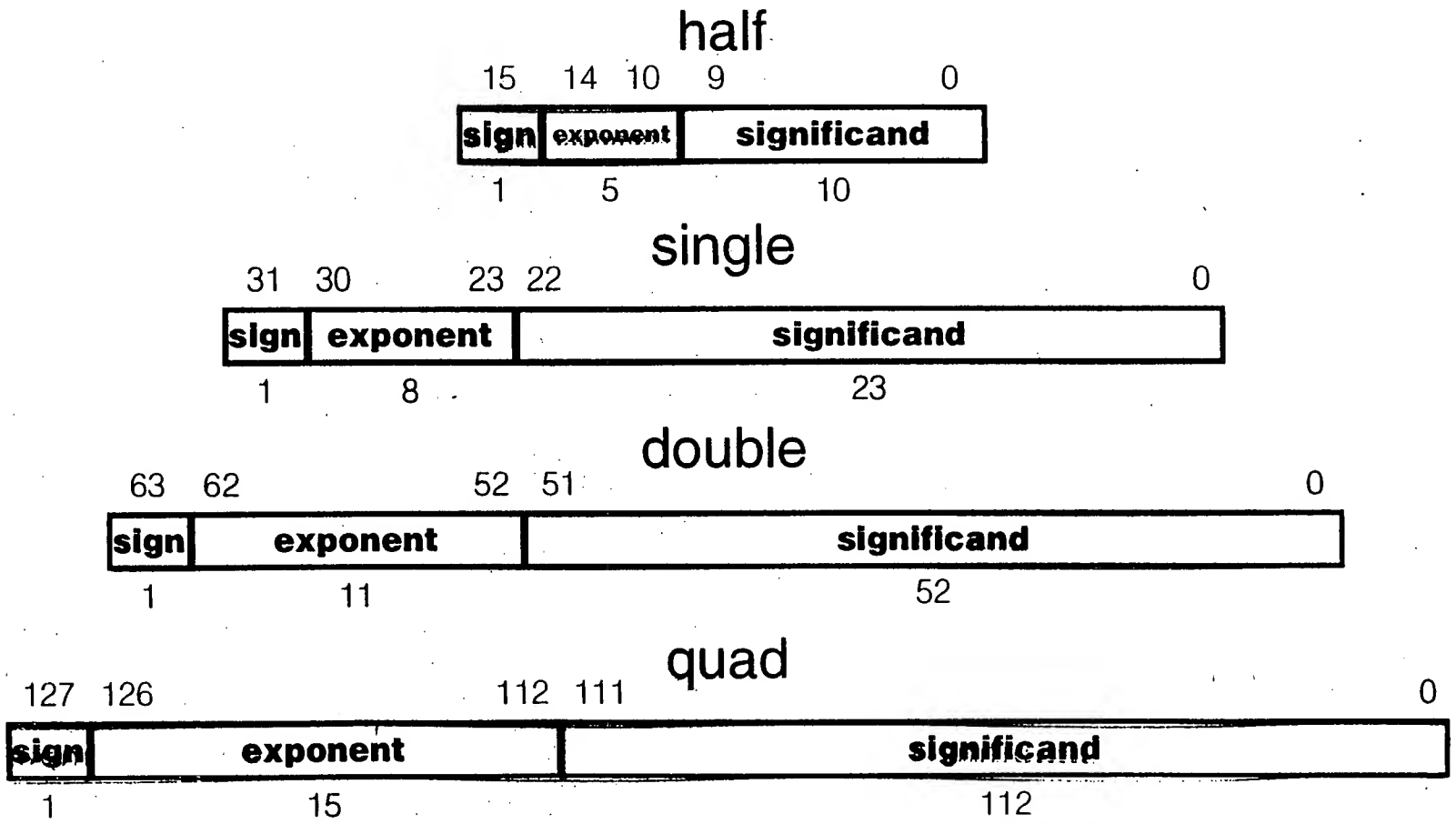


Figure 9(c)

Fixed-Point Data Sizes

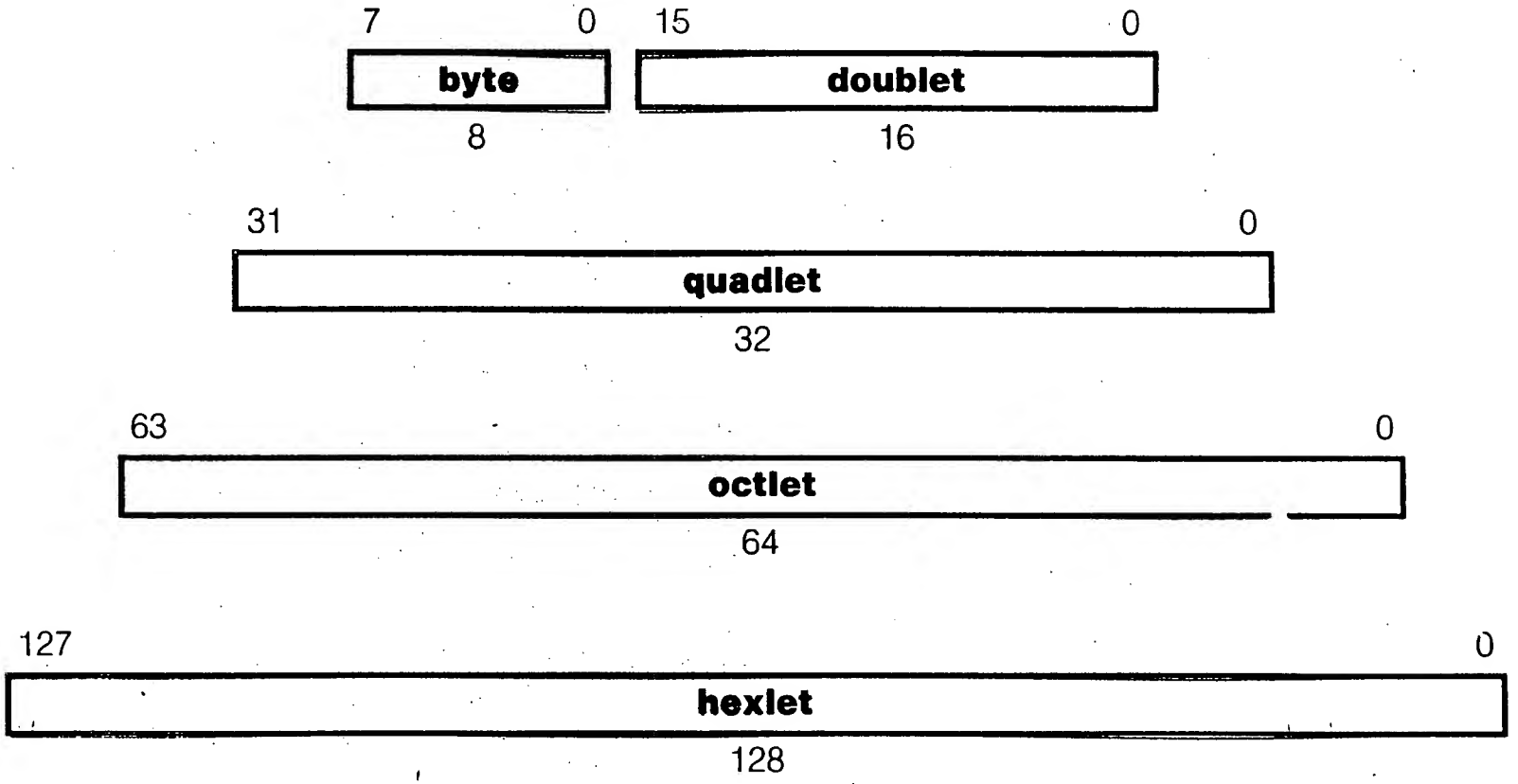


Figure 10(a)

Translation Block Diagram

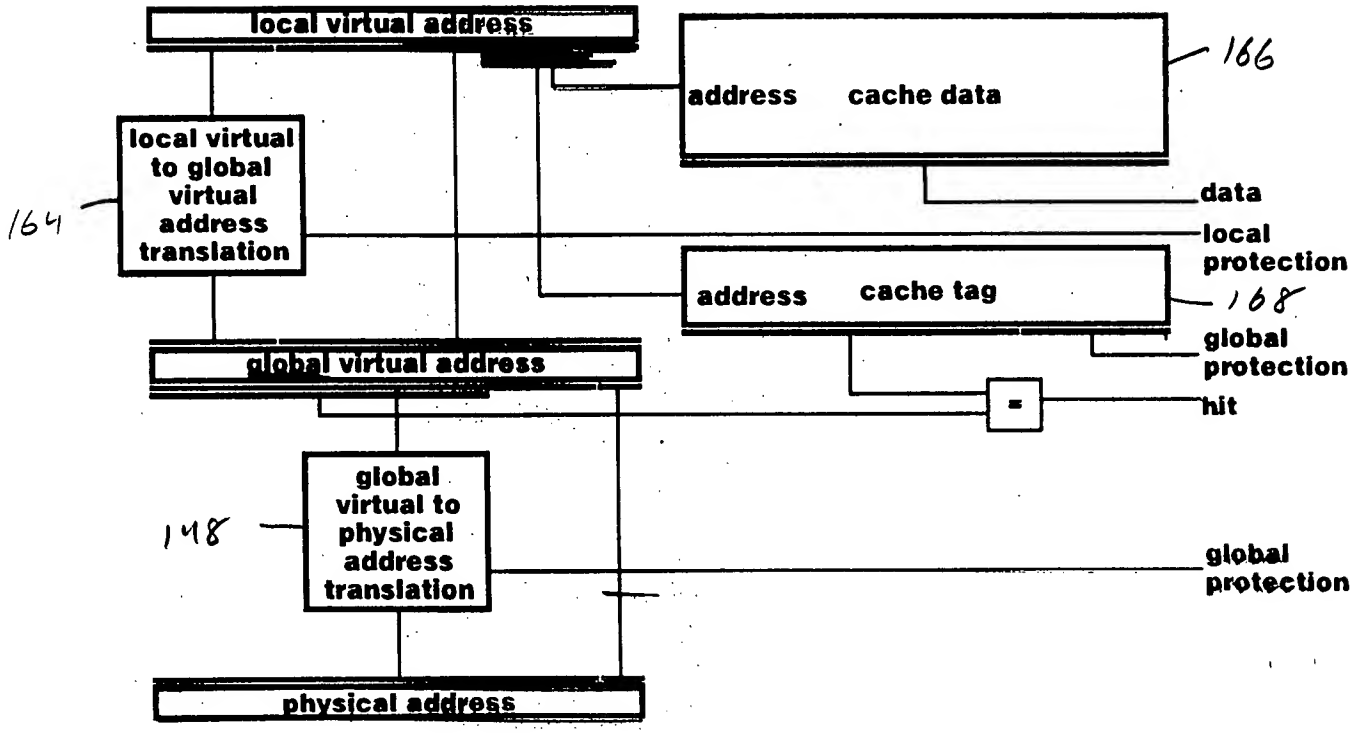


Figure 10(b)

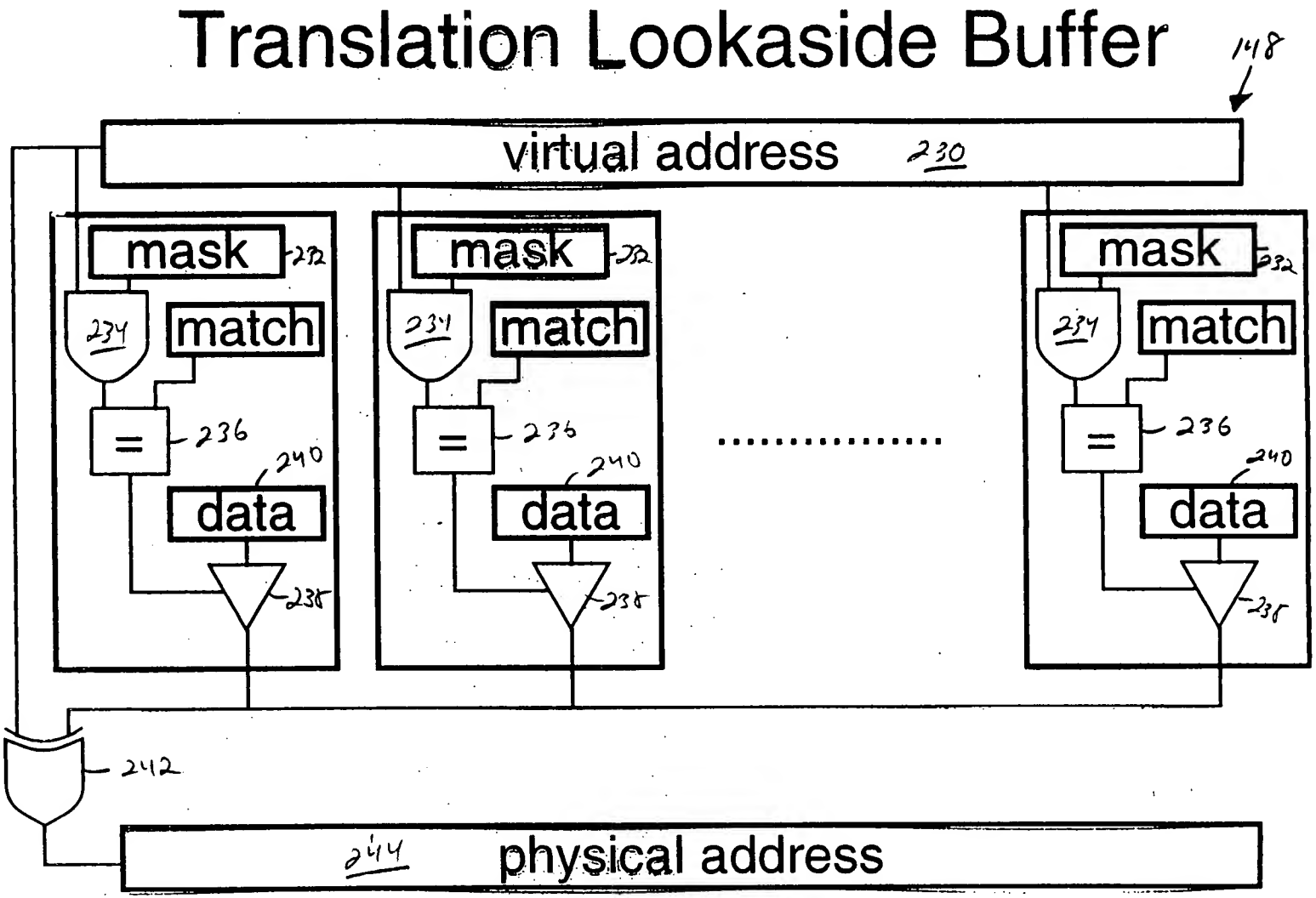


Figure 11

Superstring Pipeline

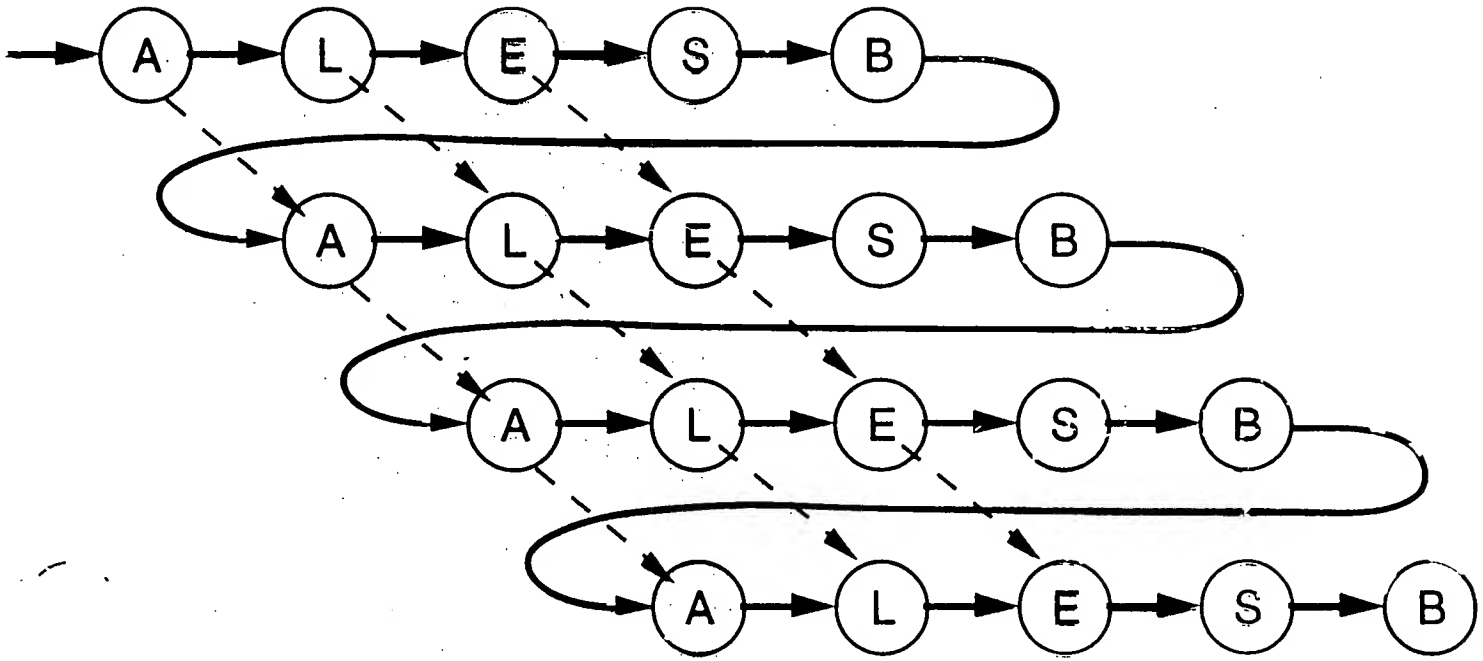


Figure 12

Superspring Pipeline

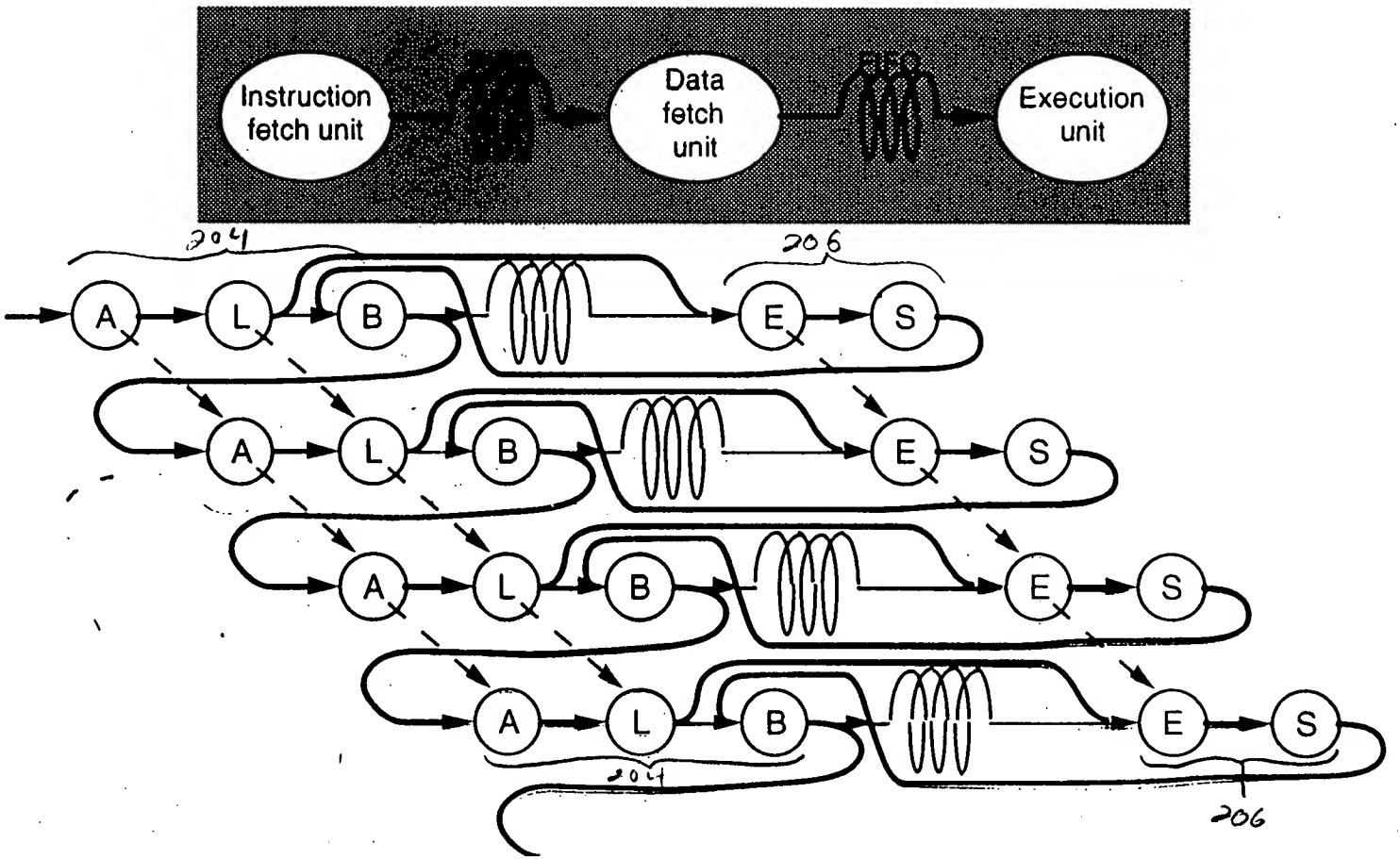


Figure 13

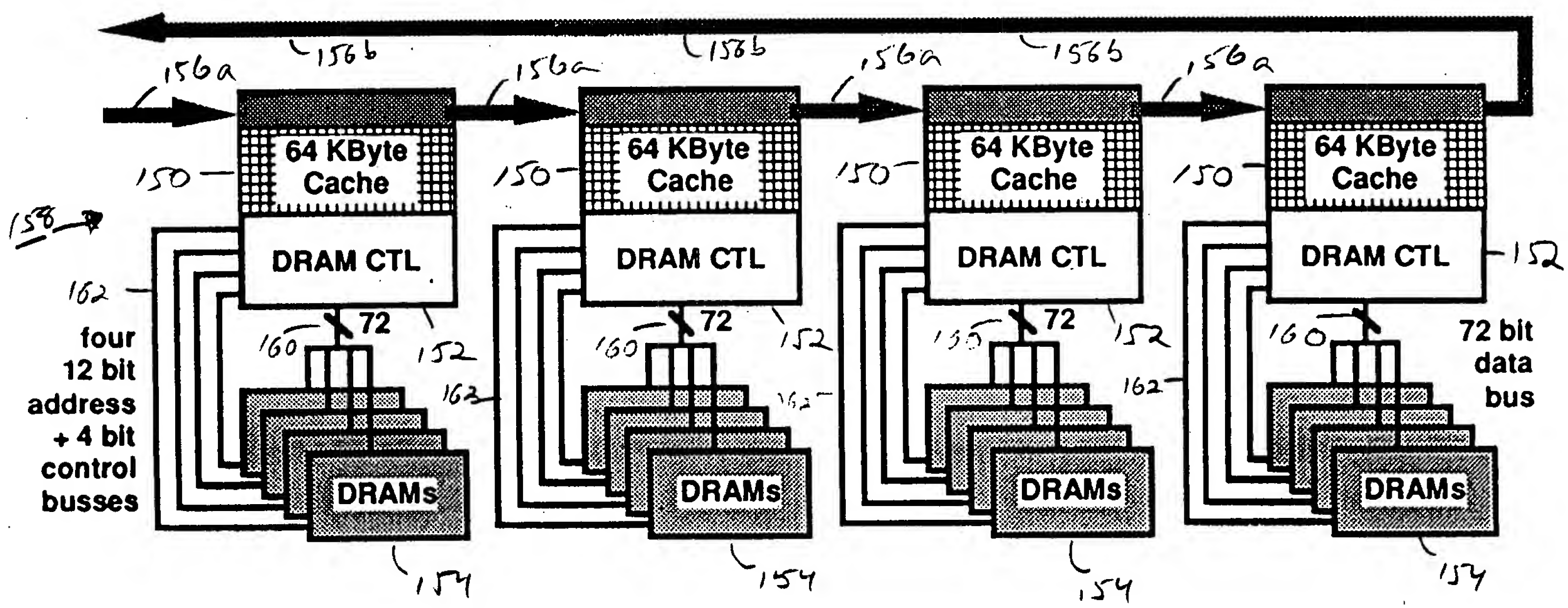
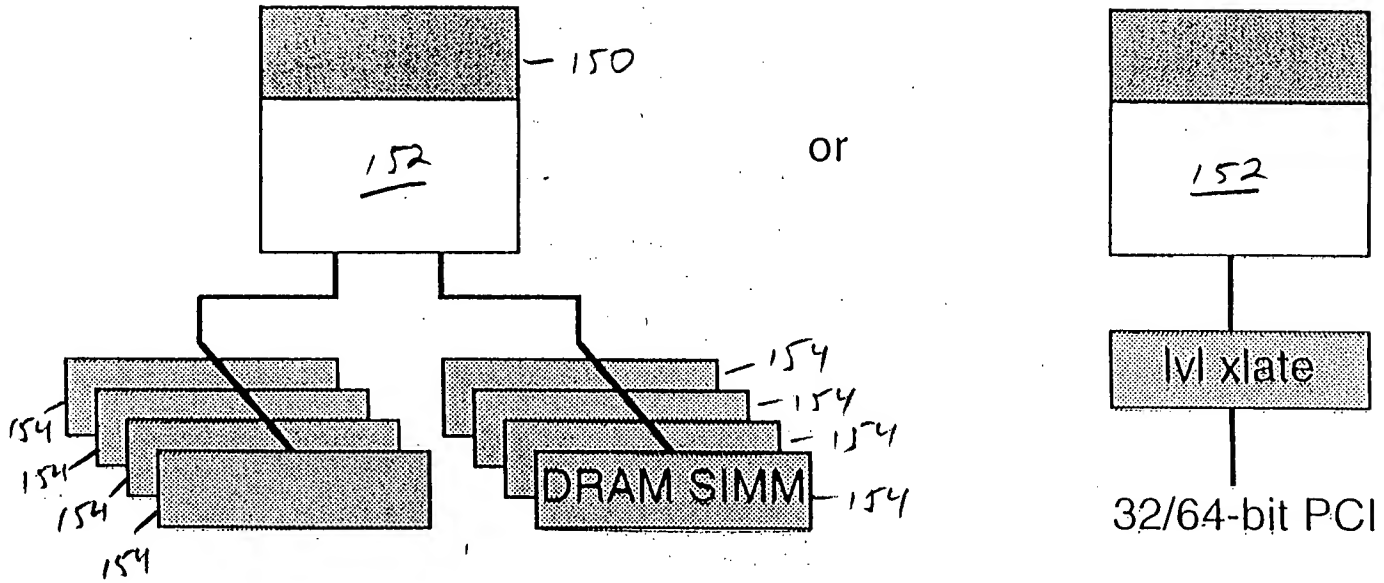


Figure 14



152
200
skew calibrator
PLL
202
194
196
192
188
190
D_{0i}
D_{7i}
CLK_i
172
174
18 bits data
178
180
D_0
$\overline{D_0}$
D_7
$\overline{D_7}$
CLK
$\overline{CLK}$
141
186
156a
D_{00}
170
176
D_{78}
CLK_0
182

Figure 15

Figure 16(a)

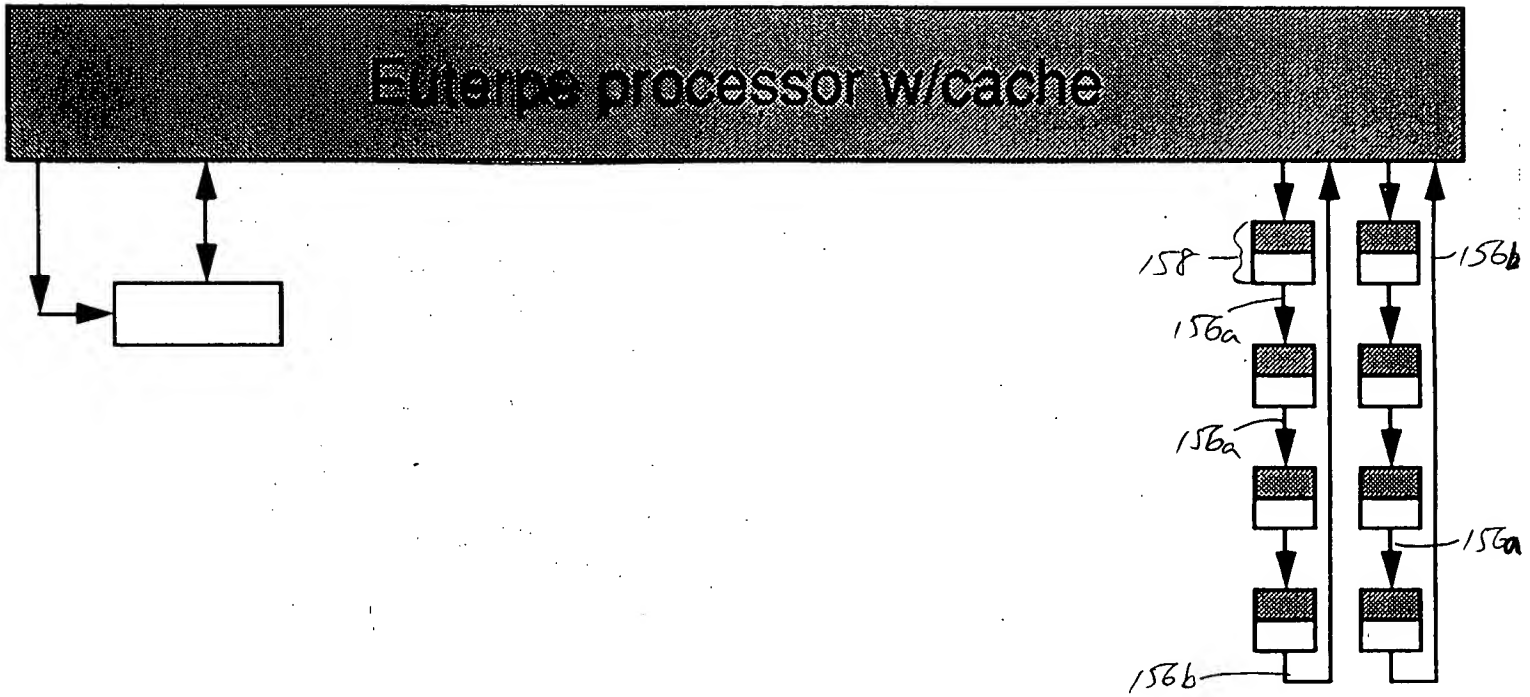


Figure 16(b)

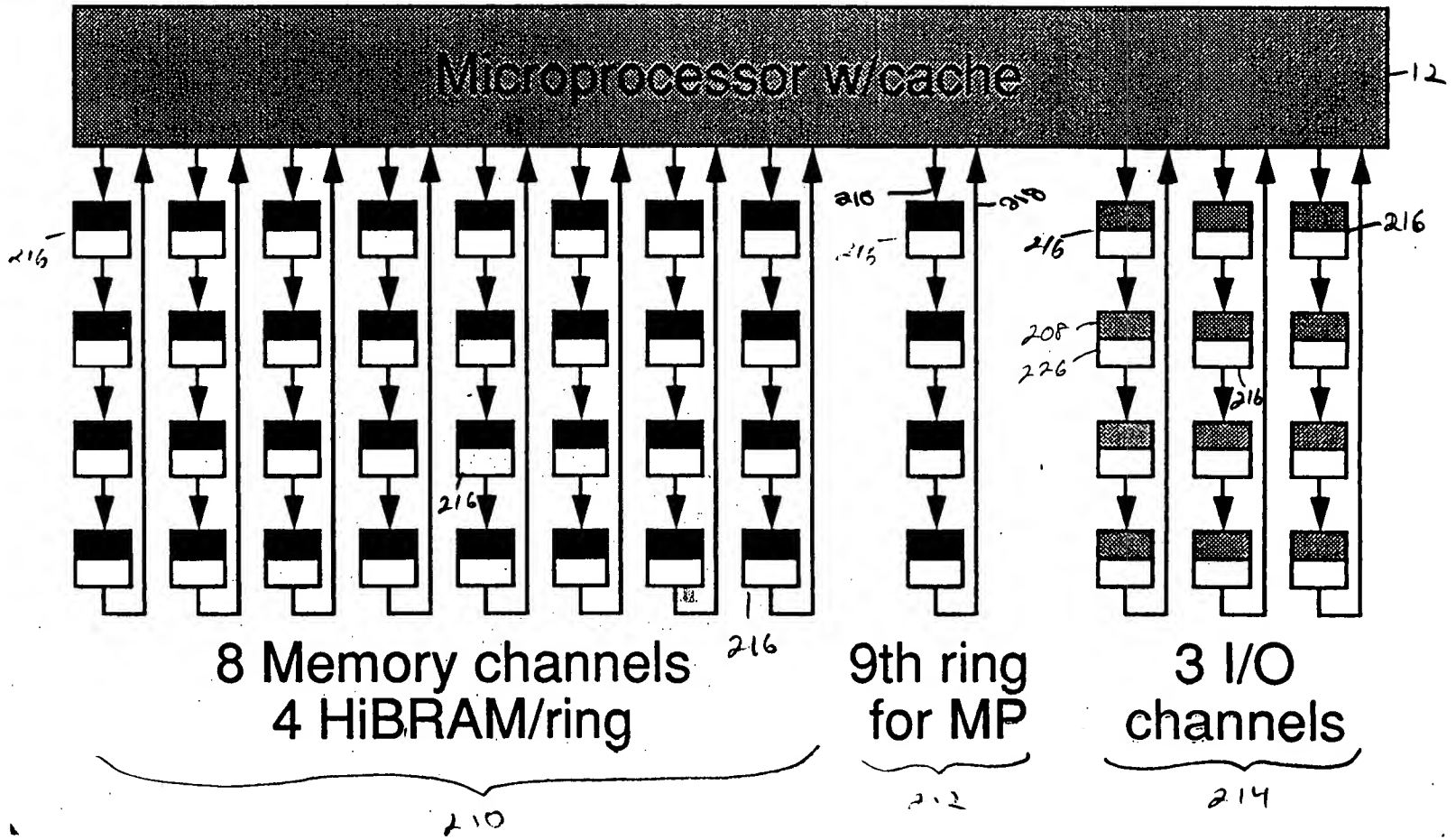


Figure 17

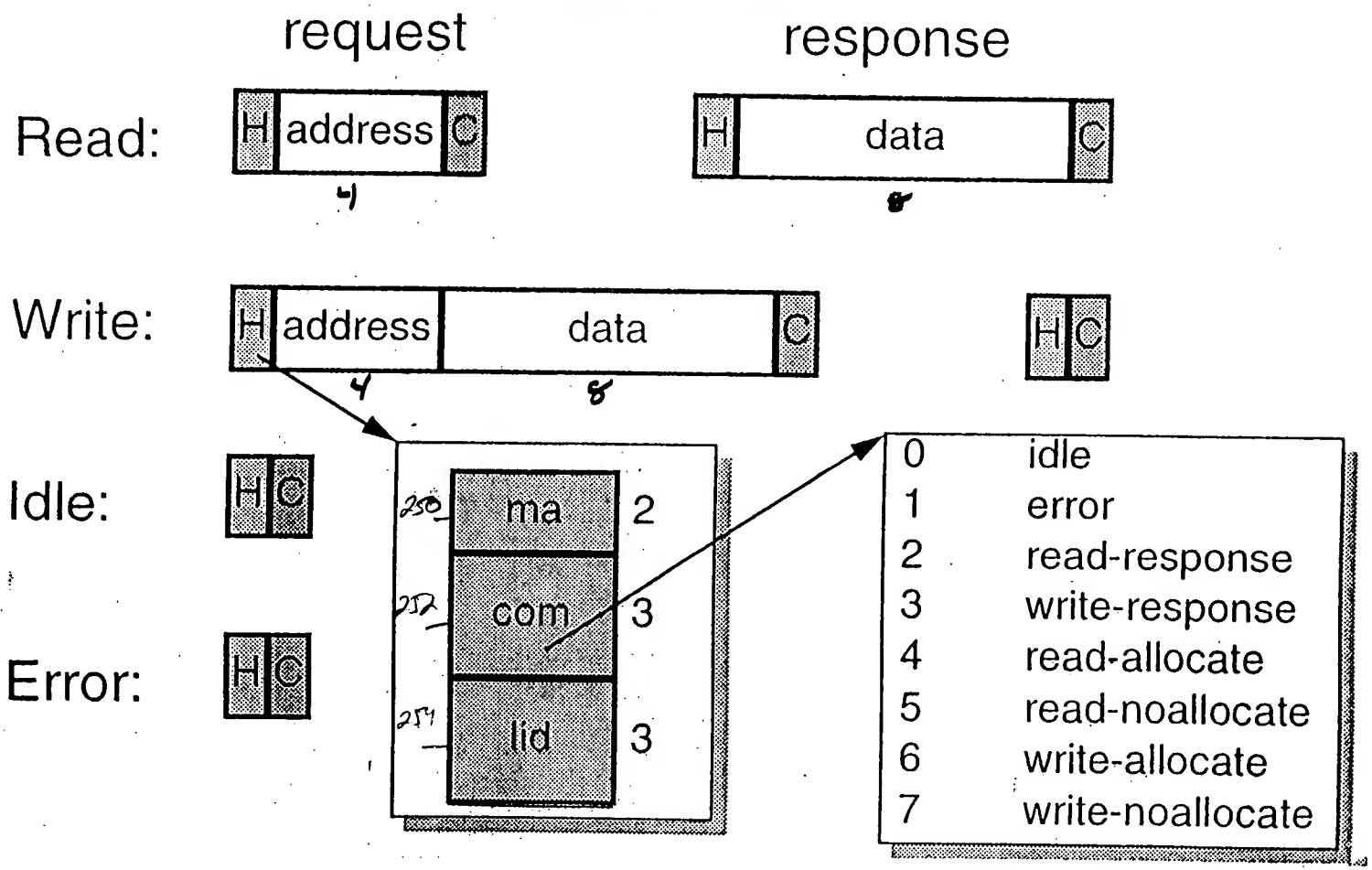
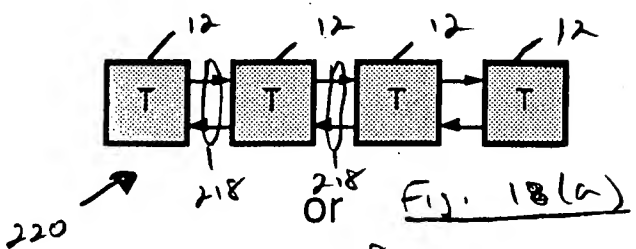


Figure 18



or

Fig. 18(a)

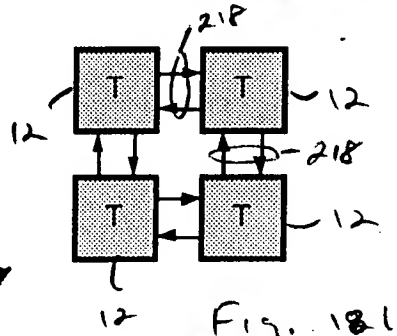


Fig. 18(b)

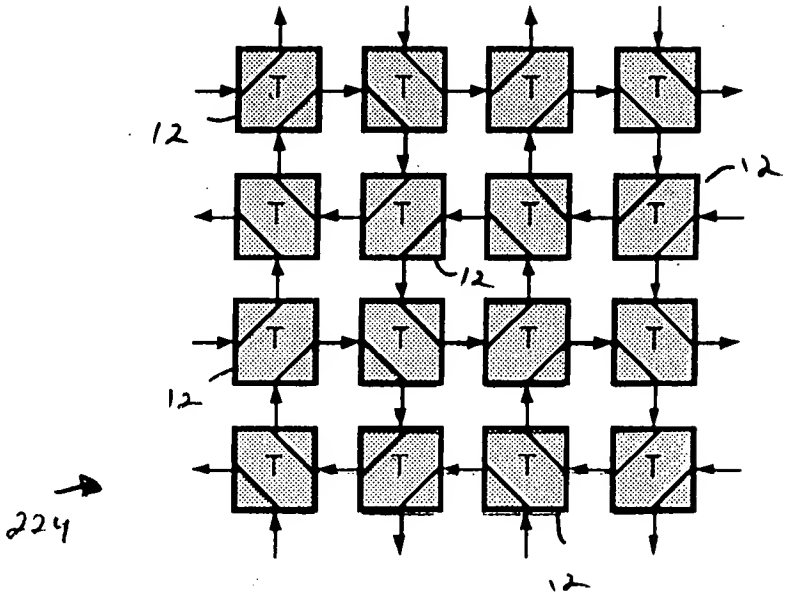
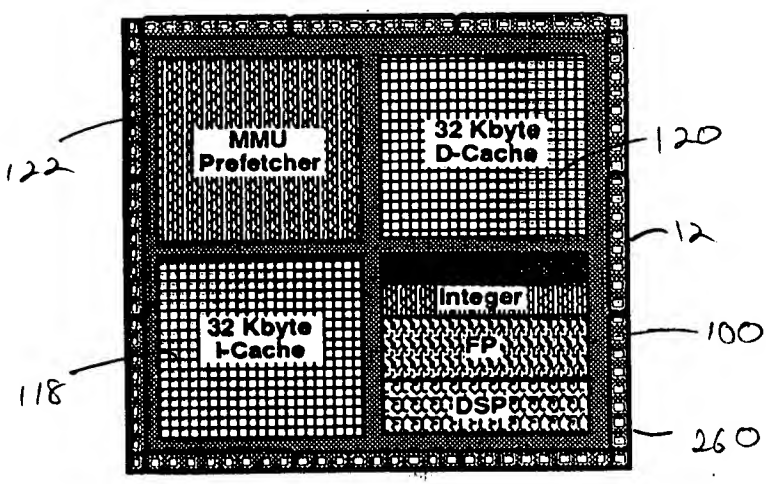
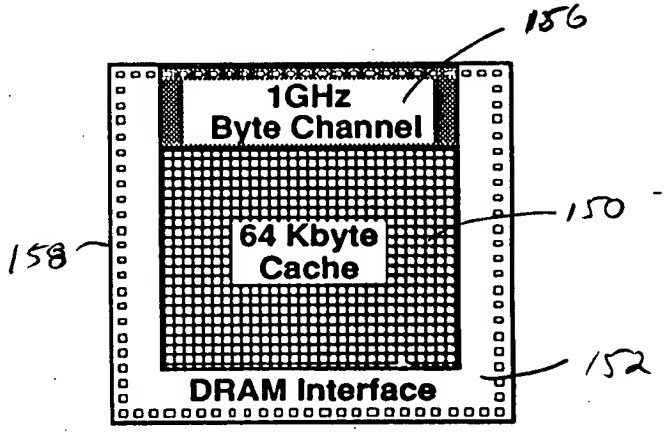


Fig. 18(c)

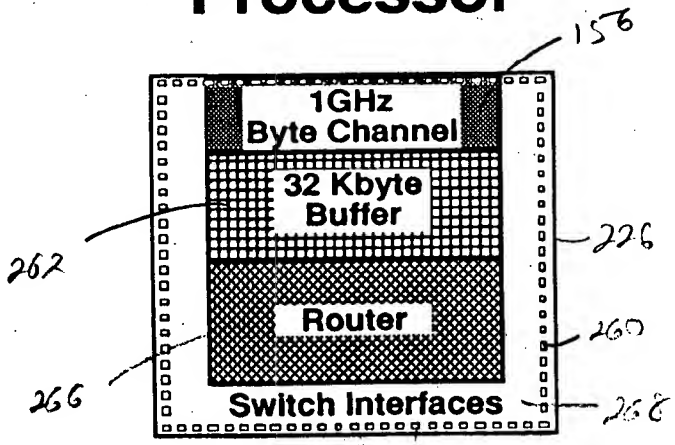
Figure 19



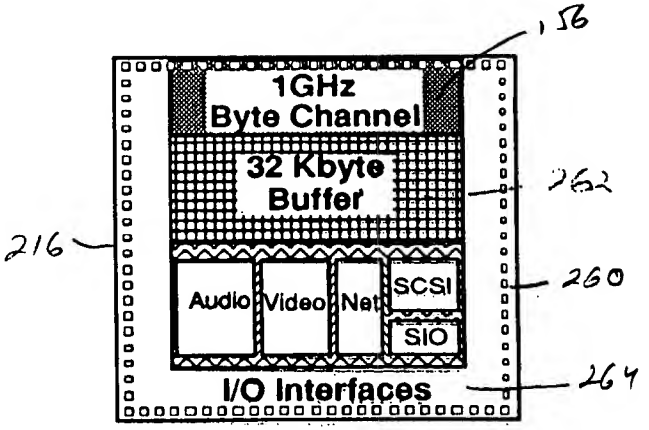
Processor



Memory



Switch



I/O